

# MSKSEMI

SEMICONDUCTOR



ESD



TVS



TSS



MOV



GDT



PLED

Product data sheet

**Product Summary**

- $V_{DS}$  30V
- $I_D$  60A
- $R_{DS(ON)}$ ( at  $V_{GS}=10V$ ) <9.0mohm
- $R_{DS(ON)}$ ( at  $V_{GS}=4.5V$ ) <11.0mohm
- 100% UIS Tested
- 100%  $\nabla V_{DS}$  Tested

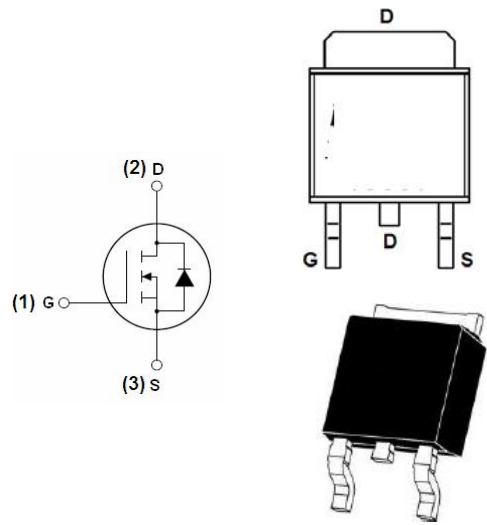
**General Description**

- Trench Power LV MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low  $R_{DS(ON)}$

**Applications**

- High current load applications
- Load switching
- Hard switched and high frequency circuits
- Uninterruptible power supply

**Schematic diagram**



TO-252

**■ Absolute Maximum Ratings** ( $T_A=25^{\circ}C$  unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		$V_{DS}$	30	V
Gate-source Voltage		$V_{GS}$	$\pm 20$	V
Drain Current	$T_C=25^{\circ}C$	$I_D$	60	A
	$T_C=100^{\circ}C$		35	
Pulsed Drain Current <sup>A</sup>		$I_{DM}$	150	A
Total Power Dissipation	$T_C=25^{\circ}C$	$P_D$	34	W
	$T_C=100^{\circ}C$		17	W
Single Pulse Avalanche Energy <sup>B</sup>		$E_{AS}$	80	mJ
Thermal Resistance Junction-to-Case <sup>C</sup>		$R_{\theta JC}$	4.4	$^{\circ}C/W$
Junction and Storage Temperature Range		$T_J, T_{STG}$	-55~+175	$^{\circ}C$

**■ Electrical Characteristics** ( $T_J=25^{\circ}\text{C}$  unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	30			V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=30V, V_{GS}=0V$	$T_J=25^{\circ}\text{C}$		1	$\mu A$
			$T_J=55^{\circ}\text{C}$		5	
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}= \pm 20V, V_{DS}=0V$			$\pm 100$	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0	1.5	2.5	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=15A$		6.5	9.0	m $\Omega$
		$V_{GS}=4.5V, I_D=15A$		8.6	11.0	
Diode Forward Voltage	$V_{SD}$	$I_S=15A, V_{GS}=0V$		0.85	1.2	V
Maximum Body-Diode Continuous Current	$I_S$				50	A
<b>Dynamic Parameters</b>						
Input Capacitance	$C_{iss}$	$V_{DS}=15V, V_{GS}=0V, f=1\text{MHz}$		920		pF
Output Capacitance	$C_{oss}$			198		
Reverse Transfer Capacitance	$C_{rss}$			114		
<b>Switching Parameters</b>						
Total Gate Charge	$Q_g$	$V_{GS}=10V, V_{DS}=15V, I_D=50A$		28		nC
Gate-Source Charge	$Q_{gs}$			7		
Gate-Drain Charge	$Q_{gd}$			5		
Reverse Recovery Charge	$Q_{rr}$	$I_F=20A, di/dt=100A/\mu s$		25		ns
Reverse Recovery Time	$t_{rr}$			26		
Turn-on Delay Time	$t_{D(on)}$	$V_{GS}=10V, V_{DD}=20V, I_D=2A, R_L=1\Omega$ $R_{GEN}=3\Omega$		8		ns
Turn-on Rise Time	$t_r$			15		
Turn-off Delay Time	$t_{D(off)}$			27		
Turn-off fall Time	$t_f$			7		

 A. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty cycle  $\leq 2\%$ .

 B.  $T_J=25^{\circ}\text{C}$ ,  $V_{DD}=20V$ ,  $V_G=10V$ ,  $L=0.5\text{mH}$ ,  $R_g=25\Omega$ 

 C.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design, while  $R_{\theta JA}$  is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

■ Typical Performance Characteristics

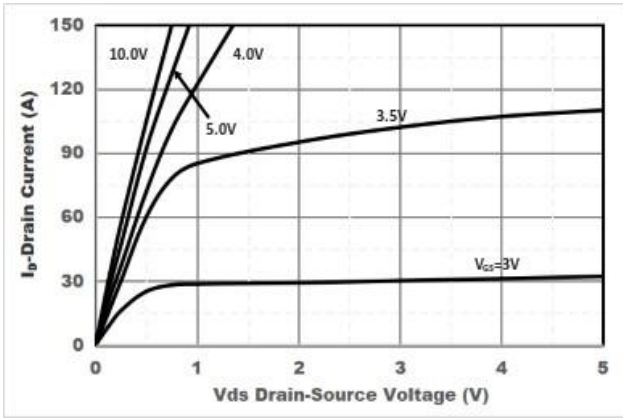


Figure1. Output Characteristics

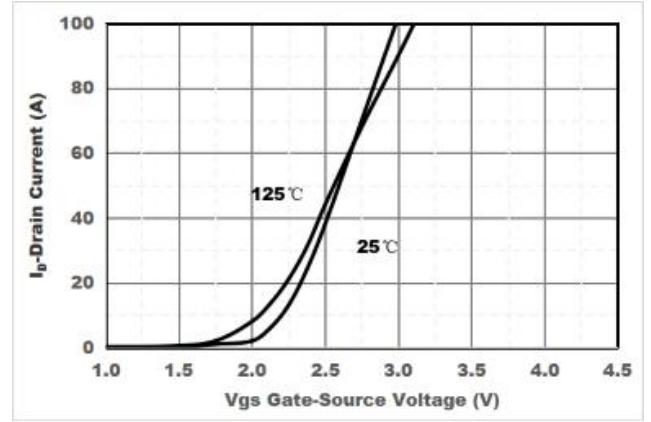


Figure2. Transfer Characteristics

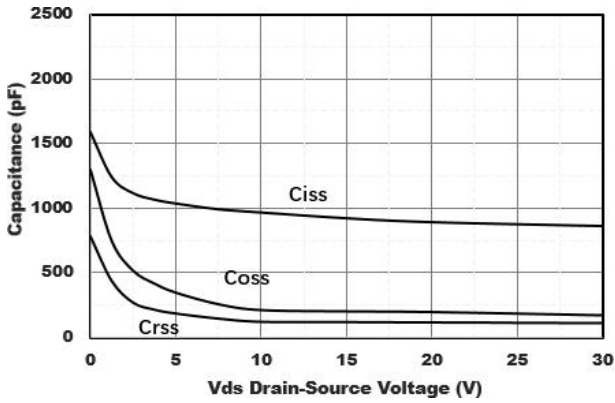


Figure3. Capacitance Characteristics

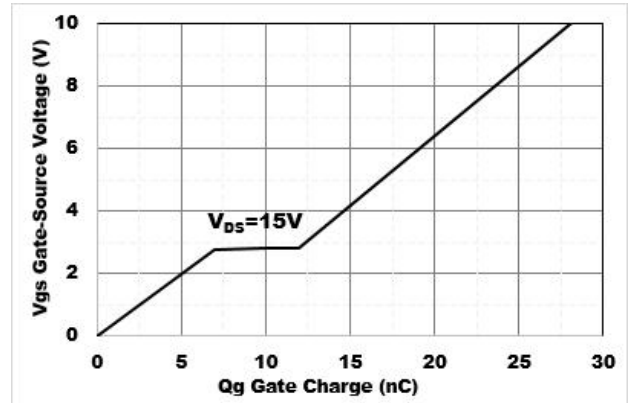


Figure4. Gate Charge

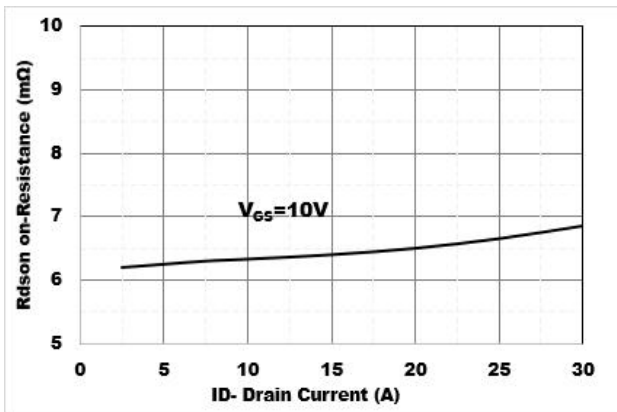


Figure5. Drain-Source on Resistance

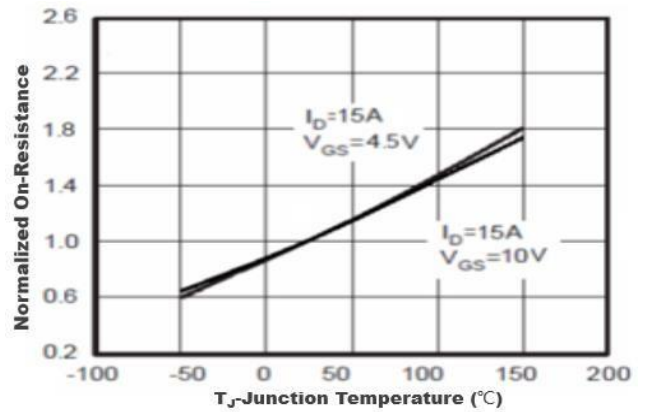


Figure6. Drain-Source on Resistance

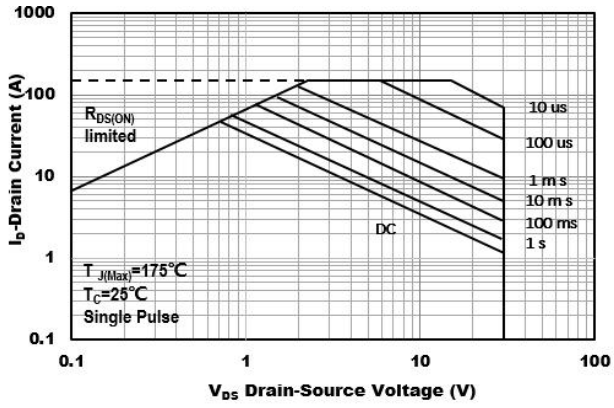


Figure7. Safe Operation Area

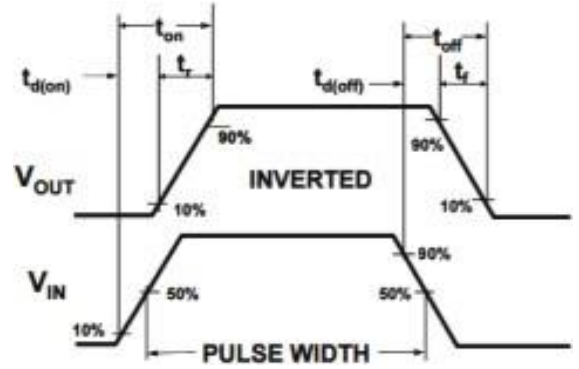
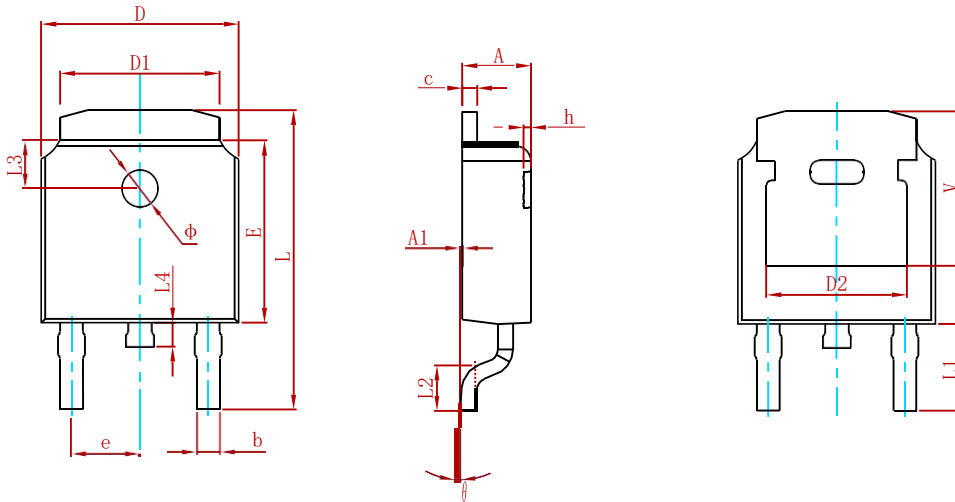


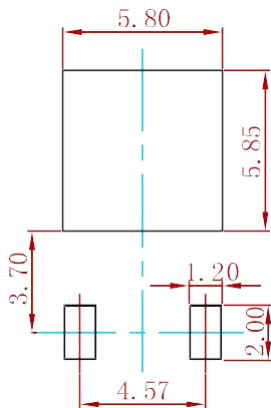
Figure8. Switching wave

**PACKAGE MECHANICAL DATA**



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.635	0.770	0.025	0.030
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	4.830 REF.		0.190 REF.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.712	10.312	0.382	0.406
L1	2.900 REF.		0.114 REF.	
L2	1.400	1.700	0.055	0.067
L3	1.600 REF.		0.063 REF.	
L4	0.600	1.000	0.024	0.039
Φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.250 REF.		0.207 REF.	

**Suggested Pad Layout**



Note:  
 1. Controlling dimension: in millimeters.  
 2. General tolerance: ± 0.05mm.  
 3. The pad layout is for reference purposes only.

**REEL SPECIFICATION**

P/N	PKG	QTY
MS60N03	TO-252	2500

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