

# MSKSEMI

SEMICONDUCTOR



ESD



TVS



TSS



MOV



GDT



PLED

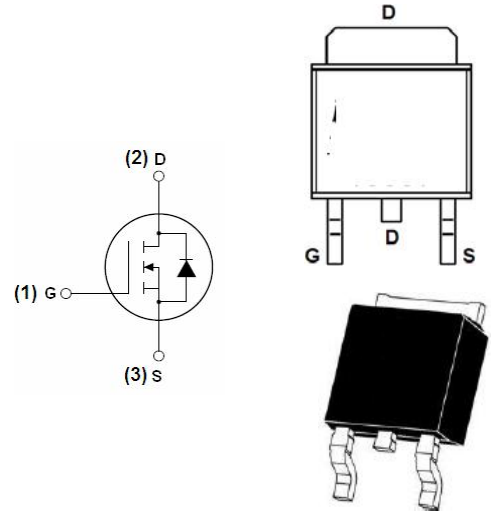
Product data sheet

**FEATURE**

- Excellent package for good heat dissipation
- Ultra low gate charge
- Low reverse transfer capacitance
- Fast switching capability
- Avalanche energy specified

VBR:100V  
RDS:70MR@10V  
ID:15A

**Schematic diagram**



TO-252

**MAXIMUM RATINGS ( T<sub>a</sub>=25°C unless otherwise noted )**

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V <sub>DS</sub>	100	V
Gate-Source Voltage	V <sub>GS</sub>	±20	V
Continuous Drain Current	I <sub>D</sub> <sup>①</sup>	15	A
Pulsed Drain Current	I <sub>DM</sub> <sup>②</sup>	60	A
Single Pulsed Avalanche Energy	E <sub>AS</sub> <sup>③</sup>	49	mJ
Power Dissipation	P <sub>D</sub> <sup>①</sup>	45	W
Thermal Resistance from Junction to Ambient	R <sub>θJA</sub> <sup>⑥</sup>	100	°C/W
Thermal Resistance from Junction to Case	R <sub>θJC</sub> <sup>①</sup>	2.78	°C/W
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55~+150	°C

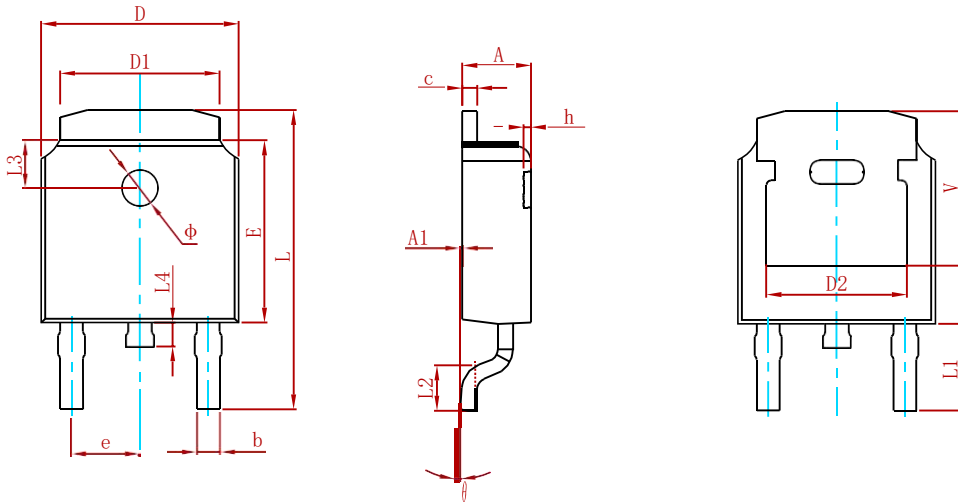
**$T_a=25\text{ }^\circ\text{C}$  unless otherwise specified**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>Off characteristics</b>						
Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	100			V
Zero gate voltage drain current	$I_{DSS}$	$V_{DS} = 80V, V_{GS} = 0V$	$T_J = 25^\circ\text{C}$		1.0	$\mu A$
			$T_J = 125^\circ\text{C}$		100	
Gate-body leakage current	$I_{GSS}$	$V_{DS} = 0V, V_{GS} = \pm 20V$			$\pm 100$	nA
<b>On characteristics</b> <sup>④</sup>						
Gate-threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	1.0	2.5	3.0	V
Static drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 8A$		70	100	m $\Omega$
<b>Dynamic characteristics</b> <sup>④ ⑤</sup>						
Input capacitance	$C_{iss}$	$V_{DS} = 25V, V_{GS} = 0V, f = 100\text{KHz}$		773	1500	pF
Output capacitance	$C_{oss}$			46	92	
Reverse transfer capacitance	$C_{rss}$			43	90	
Gate resistance	$R_g$	$f = 1\text{MHz}$		1.5		$\Omega$
<b>Switching characteristics</b> <sup>④ ⑤</sup>						
Total gate charge	$Q_g$	$V_{GS} = 10V, V_{DS} = 50V, I_D = 10A$		18	36	nC
Gate-source charge	$Q_{gs}$			2.8	5.6	
Gate-drain charge	$Q_{gd}$			7.4	14.8	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 25V, R_L = 5\Omega, V_{GS} = 10V, R_G = 1.0\Omega$		15		ns
Turn-on rise time	$t_r$			33		
Turn-off delay time	$t_{d(off)}$			41		
Turn-off fall time	$t_f$			6		
<b>Drain-Source Diode Characteristics</b>						
Drain-source diode forward voltage	$V_{SD}$ <sup>④</sup>	$V_{GS} = 0V, I_S = 8A$			1.2	V
Continuous drain-source diode forward current	$I_S$ <sup>①</sup>				15	A
Pulsed drain-source diode forward current	$I_{SM}$ <sup>②</sup>				60	A

Notes:

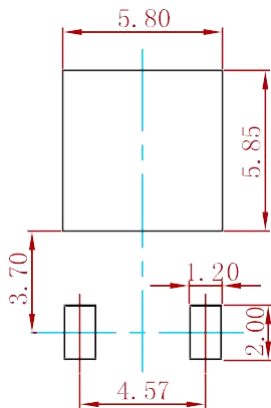
- $T_c=25^\circ\text{C}$  Limited only by maximum temperature allowed.
- $P_w \leq 10\mu s$ , Duty cycle  $\leq 1\%$ .
- EAS condition:  $V_{DD} = 25V, V_{GS} = 10V, L = 0.5\text{mH}, R_g = 25\Omega$  Starting  $T_J = 25^\circ\text{C}$ .
- Pulse Test : Pulse Width  $\leq 300\mu s$ , duty cycle  $\leq 2\%$ .
- Guaranteed by design, not subject to production.
- The value of  $R_{\theta JA}$  is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with  $T_a = 25^\circ\text{C}$ .

**PACKAGE MECHANICAL DATA**



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.635	0.770	0.025	0.030
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	4.830 REF.		0.190 REF.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.712	10.312	0.382	0.406
L1	2.900 REF.		0.114 REF.	
L2	1.400	1.700	0.055	0.067
L3	1.600 REF.		0.063 REF.	
L4	0.600	1.000	0.024	0.039
Φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.250 REF.		0.207 REF.	

**Suggested Pad Layout**



Note:  
 1. Controlling dimension: in millimeters.  
 2. General tolerance: ± 0.05mm.  
 3. The pad layout is for reference purposes only.

**REEL SPECIFICATION**

P/N	PKG	QTY
MS15N10	TO-252	2500

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