

# MSKSEMI

SEMICONDUCTOR



ESD



TVS



TSS



MOV

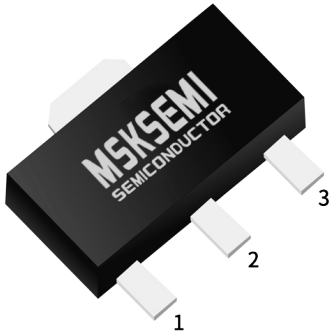


GDT



PLED

Product data sheet



SOT-89

Package	Pin assignment		
	1	2	3
SOT-89	T1	T2	G

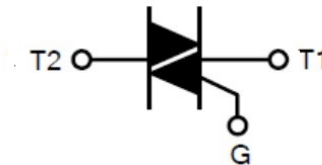
## FEATURES

- Direct interfacing to logic level ICs
- Direct interfacing to low power gate drive circuits and microcontrollers
- High blocking voltage capability
- Planar passivated for voltage ruggedness and reliability
- Triggering in all four quadrants
- Very sensitive gate

## APPLICATIONS

- General purpose bi-directional switching and phase control application.
- Air conditioner indoor fan control
- General purpose motor control
- General purpose switching

## SYMBOL:



## ABSOLUTE

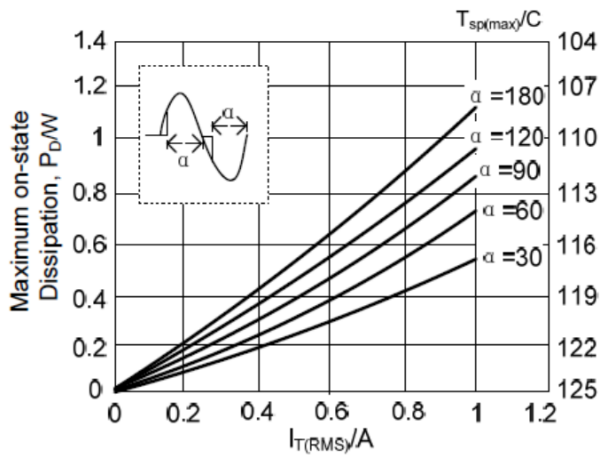
PARAMETER	SYMBOL	VALUE	UNIT	
Repetitive Peak Off-State Voltages	$V_{DRM}, V_{RRM}$	600	V	
RMS on-State Current	$I_{T(RMS)}$	1	A	
Non-Repetitive Peak On-State Current	$I_{TSM}$	16	A	
$I^2t$ for fusing	$I^2t$	1.28	A <sup>2</sup> s	
Repetitive rate of rise of on-state current after triggering	dIT/dt	I	50	A/μs
		II	50	
		III	50	
		IV	10	
Peak gate current	$I_{GM}$	2	A	
Peak Gate Voltage	$V_{GM}$	5	V	
Peak Gate Power	$P_{GM}$	5	W	
Average Gate Power	$P_{G(AV)}$	0.5	W	
Operating junction temperature	$T_J$	+125	°C	
Storage Temperature	$T_{STG}$	-40 ~ +150	°C	

**ELECTRICAL CHARACTERISTICS (T<sub>J</sub>=25°C)**

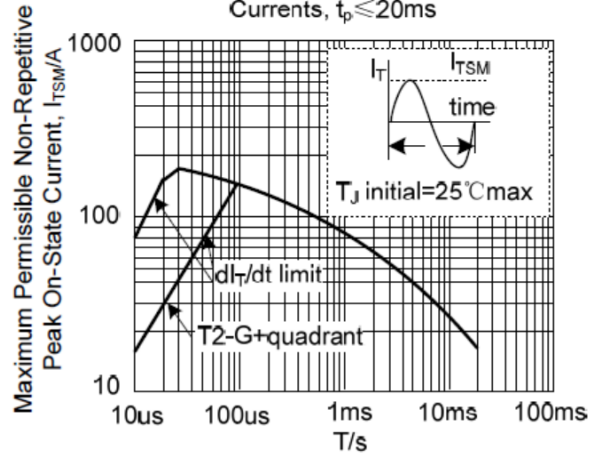
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Peak Repetitive Forward or Reverse Blocking Current	I <sub>DRM</sub> I <sub>RRM</sub>	V <sub>AK</sub> = Rated V <sub>DRM</sub> or V <sub>RRM</sub> ;		0.5	mA
Gate Trigger Current	I <sub>GT</sub>	V <sub>D</sub> =12V, R <sub>L</sub> =100Ω	I	5.0	mA
			II	5.0	
			III	5.0	
			IV	10	
Gate Trigger Voltage	V <sub>GT</sub>	V <sub>D</sub> =12V, I <sub>T</sub> =100mA		1.5	V
Peak Forward On-State Voltage	V <sub>TM</sub>	I <sub>T</sub> =2.0A		1.5	V
Latch Current	I <sub>L</sub>	V <sub>D</sub> =12V I <sub>G</sub> =0.1A,	I	5.0	mA
			II	8.0	
			III	5.0	
			IV	5.0	
Holding Current	I <sub>H</sub>	V <sub>D</sub> =12V, I <sub>G</sub> =0.1A		5	mA
Gate Non-Trigger Voltage	V <sub>GD</sub>	V <sub>D</sub> =V <sub>DRM</sub>	0.2		V
Critical Rate of Rise of Off-State Voltage	dV/dt	V <sub>D</sub> =67%V <sub>DRM</sub> , R <sub>GK</sub> =1kΩ	5		V/μs

**ELECTRICAL CHARACTERISTIC CURVE**

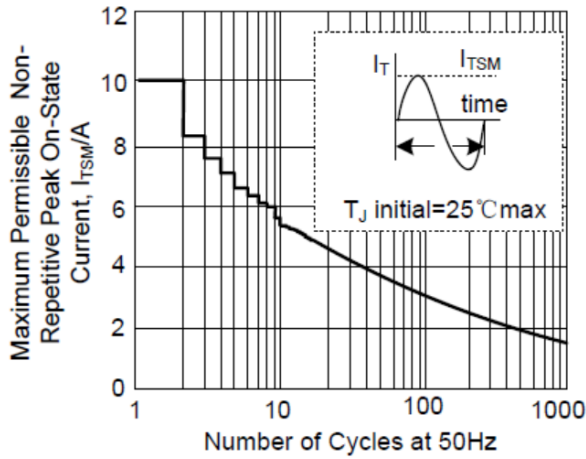
Maximum on-state Dissipation vs. RMS On-state Current, I<sub>T(RMS)</sub>, Where α =conduction Angle



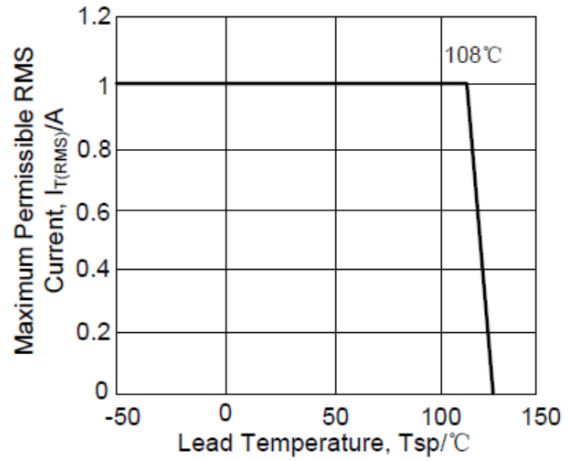
Maximum Permissible Non-repetitive Peak On-state Current vs. Pulse Width t<sub>p</sub>, for Sinusoidal Currents, t<sub>p</sub> ≤ 20ms



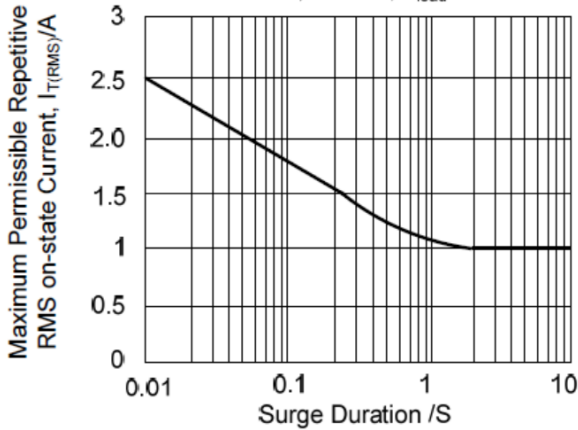
Maximum Permissible Non-Repetitive Peak On-State Current vs. Number of Cycles, for Sinusoidal Currents



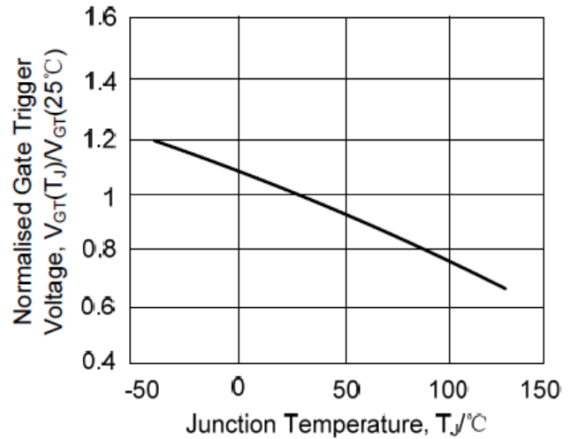
Maximum Permissible RMS Current  $I_{T(RMS)}$  vs. Lead Temperature



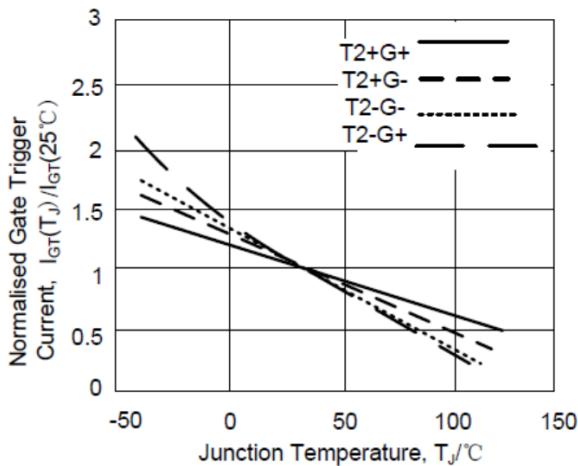
Maximum Permissible Repetitive RMS on-state Current vs. Surge Duration, for Sinusoidal Currents,  $f=50Hz$ ;  $T_{lead} \leq 51°C$



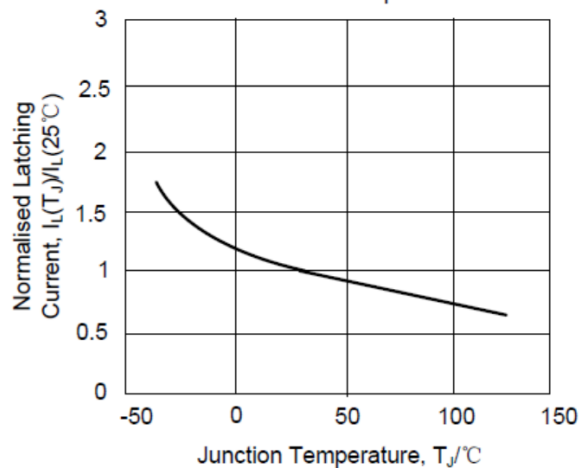
Normalised Gate Trigger Voltage vs. Junction Temperature

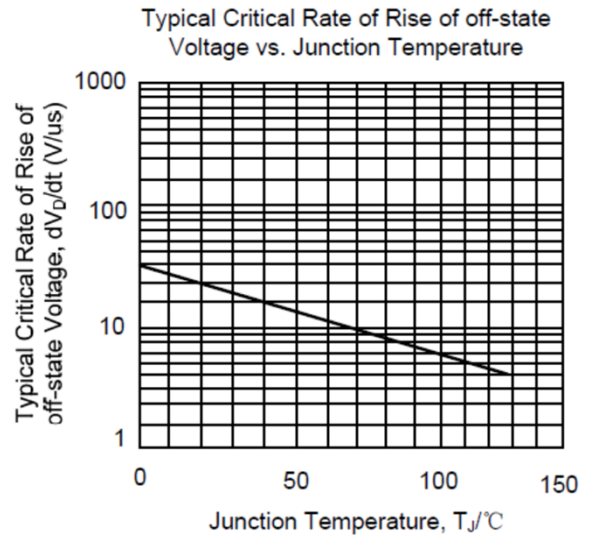
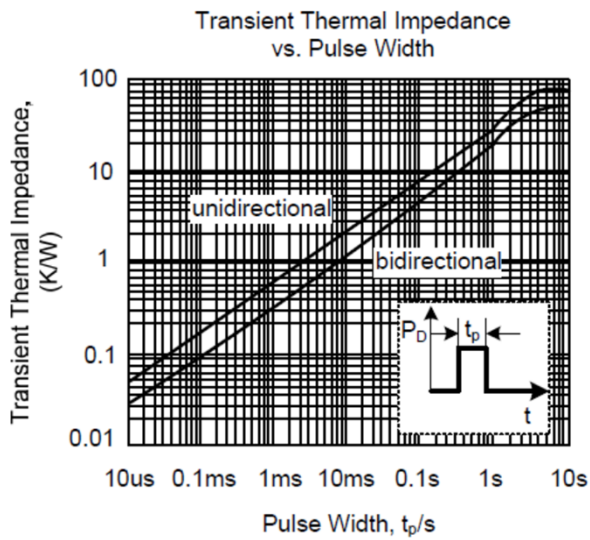
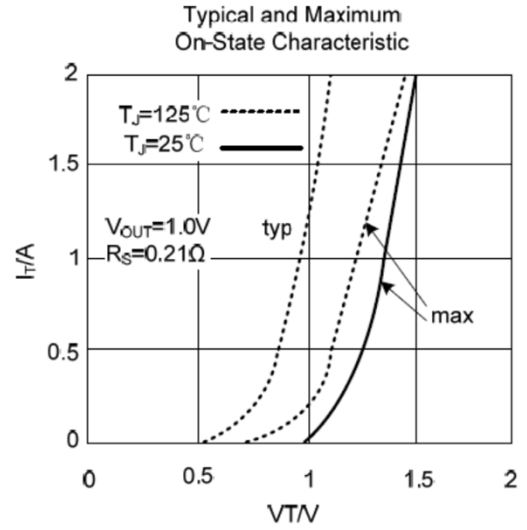
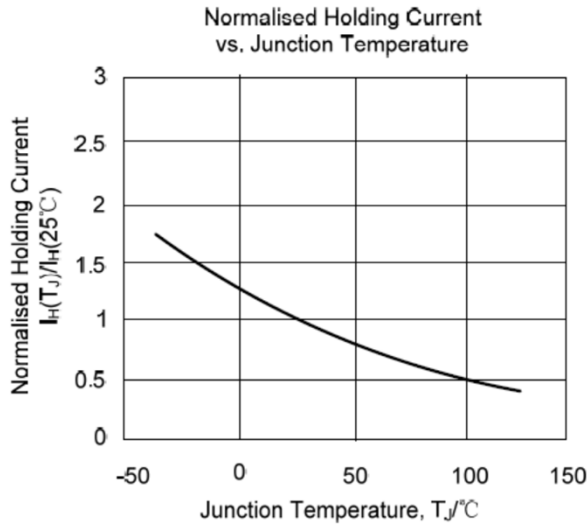


Normalised Gate Trigger Current vs. Junction Temperature

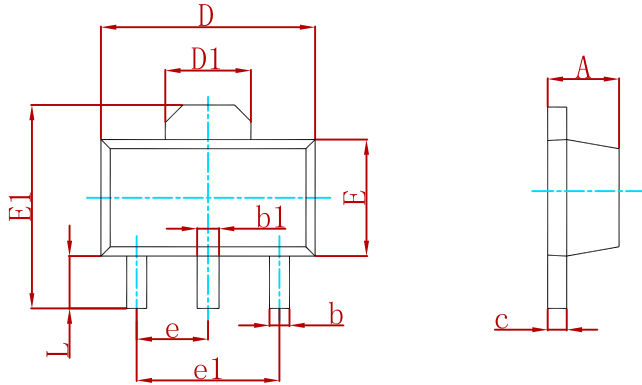


Normalised Latching Current vs. Junction Temperature



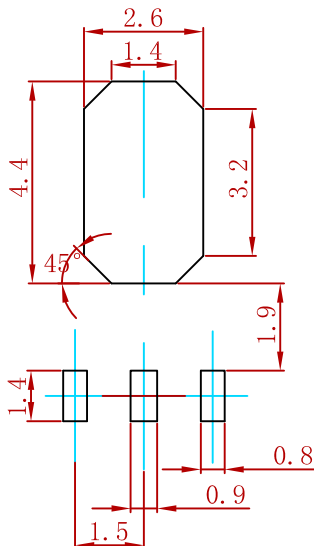


**PACKAGE MECHANICAL DATA**



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.400	1.600	0.055	0.063
b	0.320	0.520	0.013	0.020
b1	0.400	0.580	0.016	0.023
c	0.350	0.440	0.014	0.017
D	4.400	4.600	0.173	0.181
D1	1.550 REF.		0.061 REF.	
E	2.300	2.600	0.091	0.102
E1	3.940	4.250	0.155	0.167
e	1.500 TYP.		0.060 TYP.	
e1	3.000 TYP.		0.118 TYP.	
L	0.900	1.200	0.035	0.047

**Suggested Pad Layout**



Note:  
 1. Controlling dimension: in millimeters.  
 2. General tolerance: ±0.05mm.  
 3. The pad layout is for reference purposes only.

**REEL SPECIFICATION**

P/N	PKG	QTY
BT131-600	SOT-89	1000

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