

# MSKSEMI

SEMICONDUCTOR



ESD



TVS



TSS



MOV



GDT

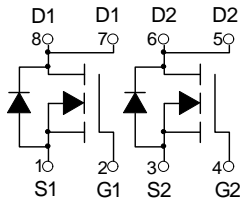


PLED

Product data sheet



SOP-8



Dual N-Channel MOSFET

**Description**

The AO4828-MS uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in a wide variety of applications.

**General Features**

- $V_{DS} = 60V, I_D = 6.5A$
- $R_{DS(ON)} < 36m\Omega @ V_{GS} = 10V$
- $R_{DS(ON)} < 48m\Omega @ V_{GS} = 4.5V$

- High density cell design for ultra low  $R_{dson}$
- Fully characterized avalanche voltage and current
- Low gate to drain charge to reduce switching losses

**Application**

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

**Absolute Maximum Ratings ( $T_A = 25^\circ C$  unless otherwise noted)**

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	60	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	6.5	A
Drain Current-Continuous( $T_C = 100^\circ C$ )	$I_D(100^\circ C)$	5	A
Pulsed Drain Current	$I_{DM}$	30	A
Maximum Power Dissipation	$P_D$	2.1	W
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 150	$^\circ C$

**Thermal Characteristic**

Thermal Resistance, Junction-to-Ambient <sup>(Note 2)</sup>	$R_{\theta JA}$	60	$^\circ C/W$
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**Electrical Characteristics (T<sub>A</sub>=25°C unless otherwise noted)**

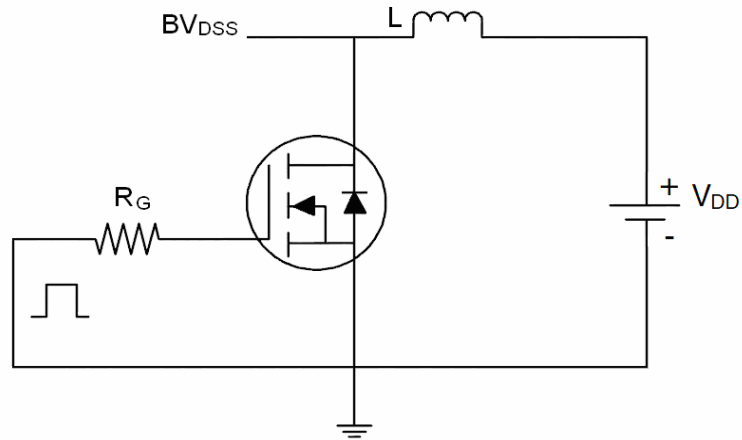
Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	60	69	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =60V, V <sub>GS</sub> =0V	-	-	1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	-	-	±100	nA
<b>On Characteristics</b> (Note 3)						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.0	1.4	2.0	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =6A		30	36	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =4A		34	48	mΩ
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =5V, I <sub>D</sub> =6A		20	-	S
<b>Dynamic Characteristics</b> (Note 4)						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V, F=1.0MHz		1920		PF
Output Capacitance	C <sub>oss</sub>			155		PF
Reverse Transfer Capacitance	C <sub>rss</sub>			116		PF
<b>Switching Characteristics</b> (Note 4)						
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DS</sub> =30V, R <sub>L</sub> =4.7Ω V <sub>GS</sub> =10V, R <sub>GEN</sub> =3Ω	-	8	-	nS
Turn-on Rise Time	t <sub>r</sub>		-	5	-	nS
Turn-Off Delay Time	t <sub>d(off)</sub>		-	29	-	nS
Turn-Off Fall Time	t <sub>f</sub>		-	6	-	nS
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =30V, I <sub>D</sub> =6A, V <sub>GS</sub> =10V	-	50	-	nC
Gate-Source Charge	Q <sub>gs</sub>		-	8	-	nC
Gate-Drain Charge	Q <sub>gd</sub>		-	16	-	nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage (Note 3)	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =6A	-	-	1.2	V
Diode Forward Current (Note 2)	I <sub>S</sub>		-	-	7	A
Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> = 25°C, I <sub>F</sub> = 7A di/dt = 100A/μs (Note 3)	-	35	-	nS
Reverse Recovery Charge	Q <sub>rr</sub>		-	43	-	nC
Forward Turn-On Time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

**Notes:**

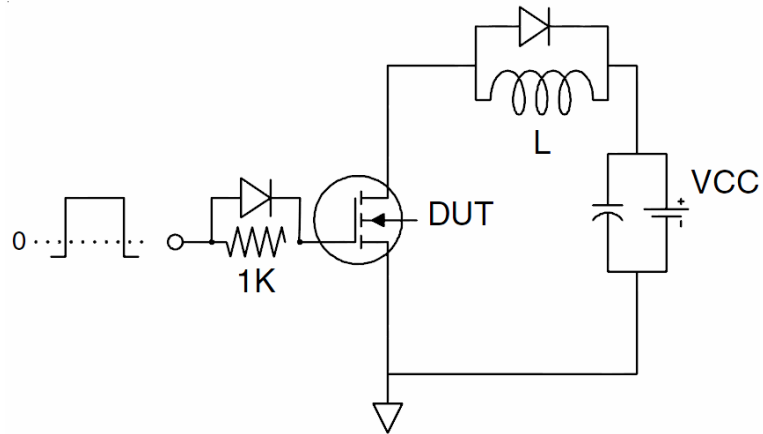
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production

**Test Circuit**

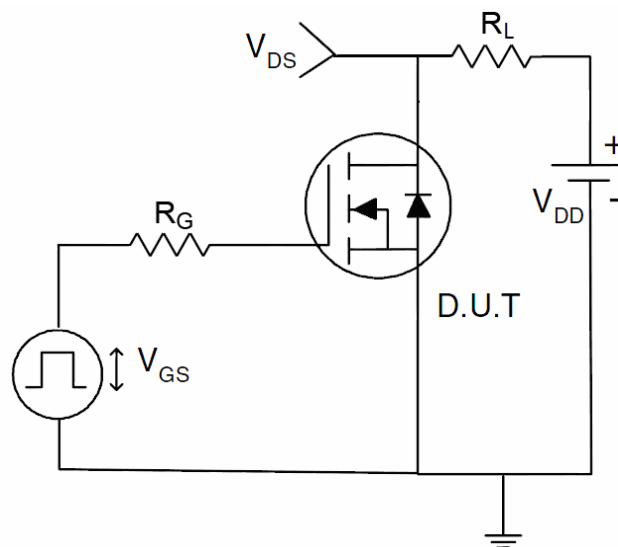
**1) EAS test Circuits**



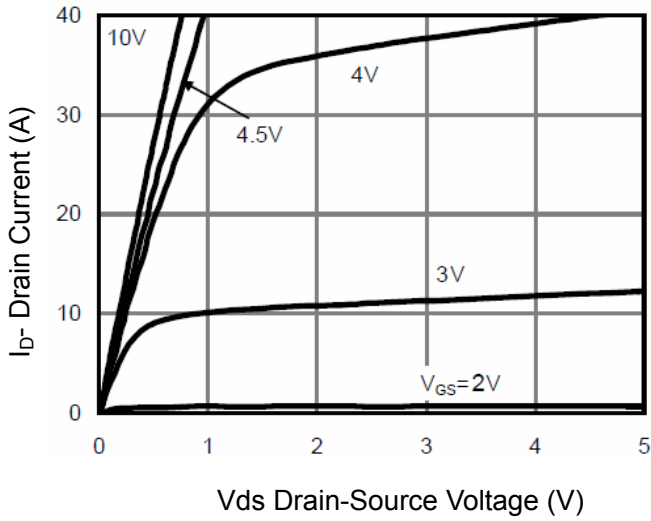
**2) Gate charge test Circuit**



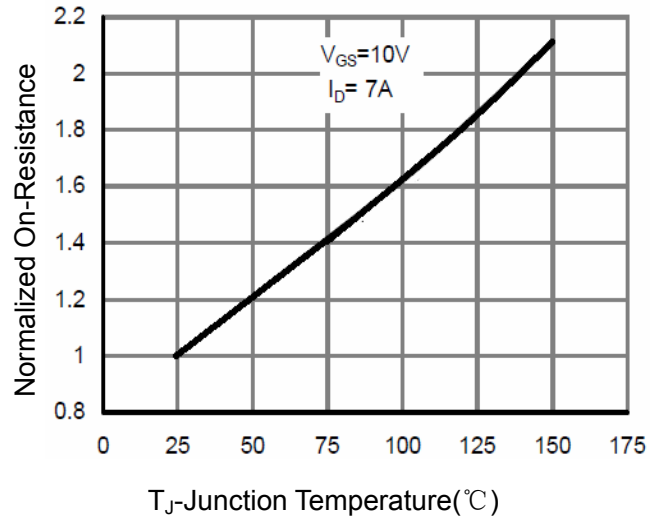
**3) Switch Time Test Circuit**



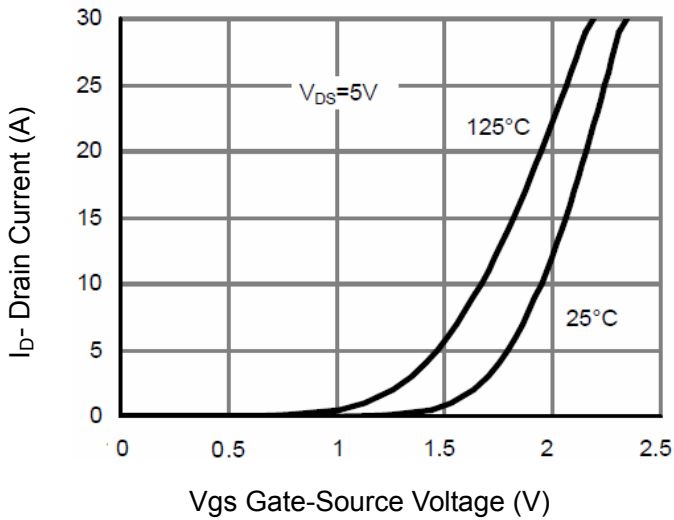
**Typical Electrical and Thermal Characteristics (Curves)**



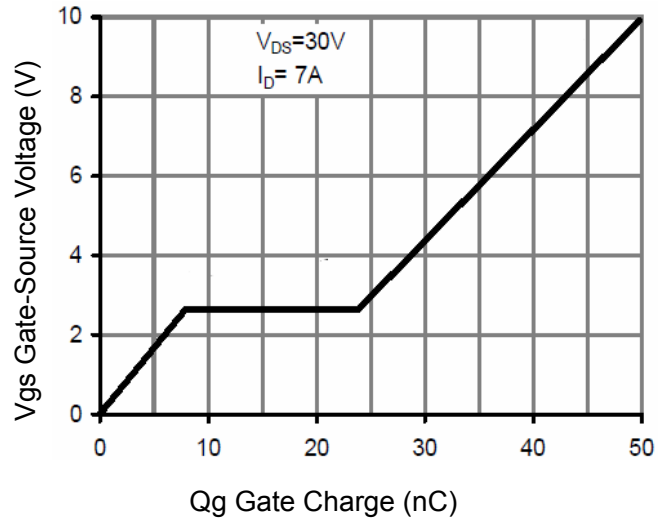
**Figure 1 Output Characteristics**



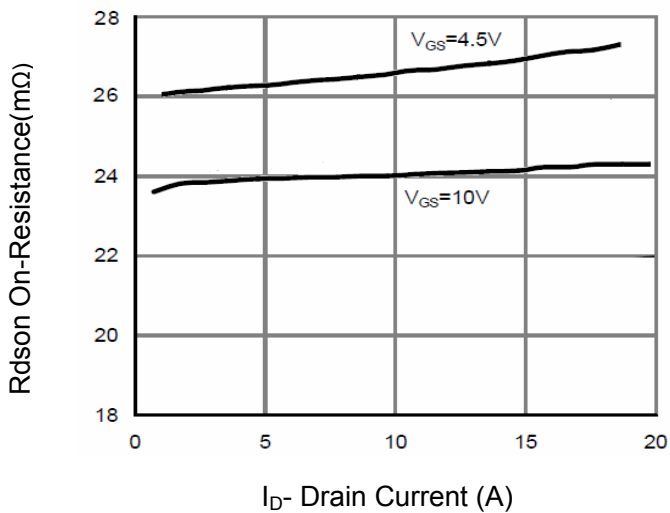
**Figure 4 Rdson-Junction Temperature**



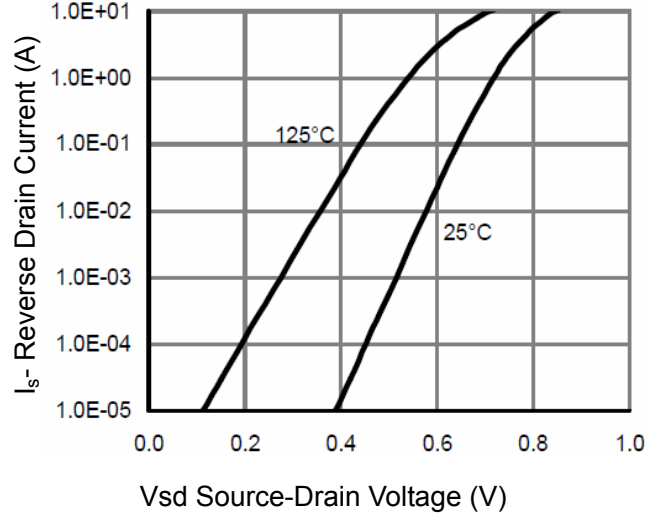
**Figure 2 Transfer Characteristics**



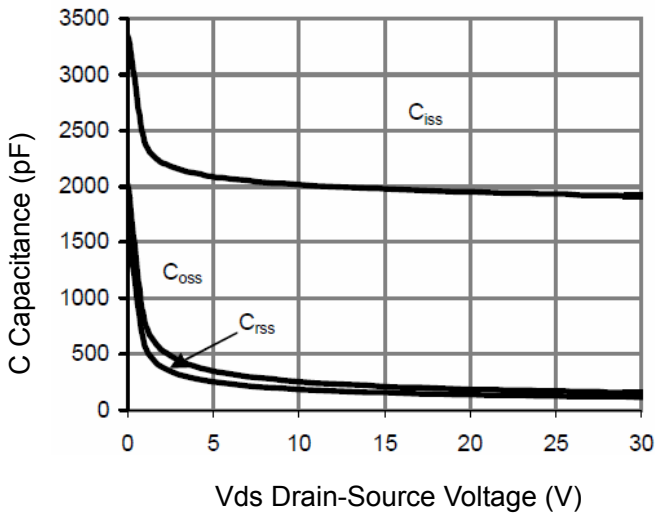
**Figure 5 Gate Charge**



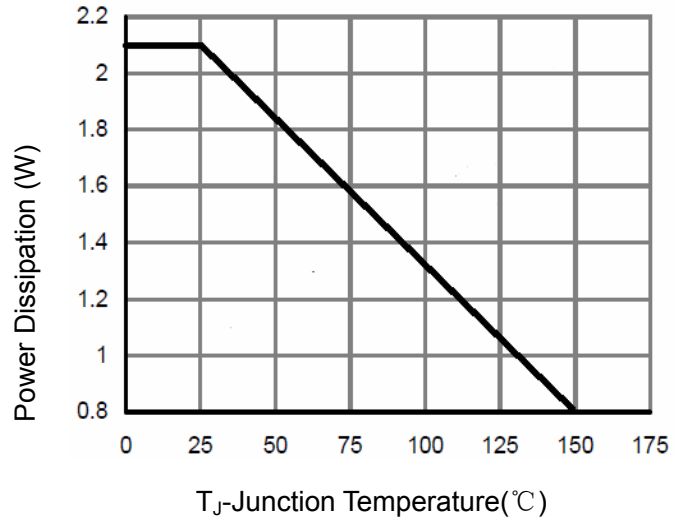
**Figure 3 Rdson- Drain Current**



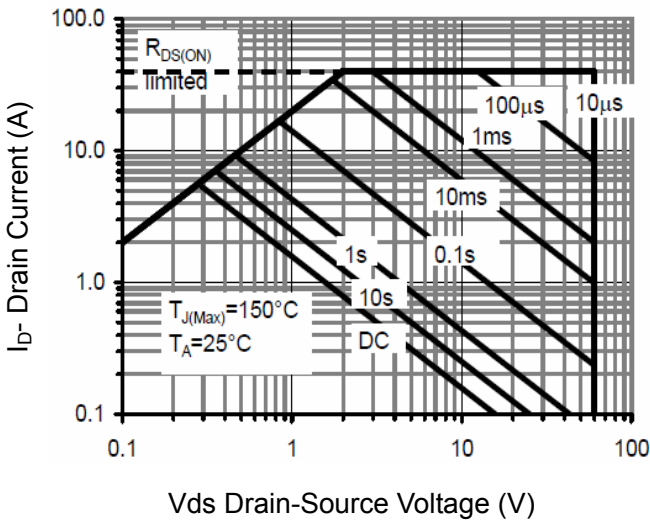
**Figure 6 Source- Drain Diode Forward**



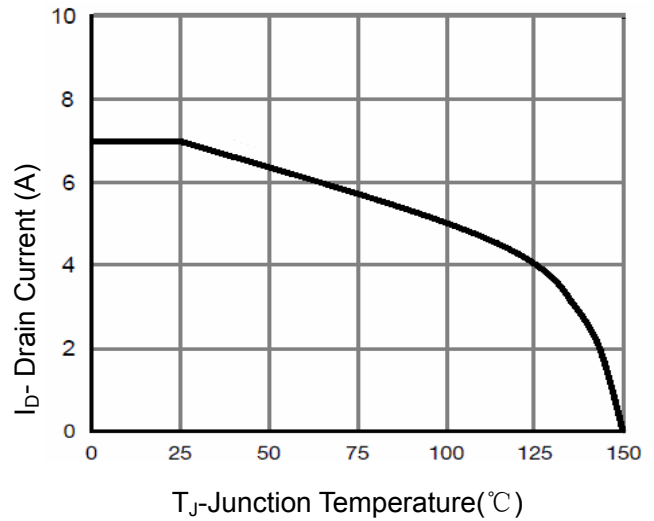
**Figure 7 Capacitance vs Vds**



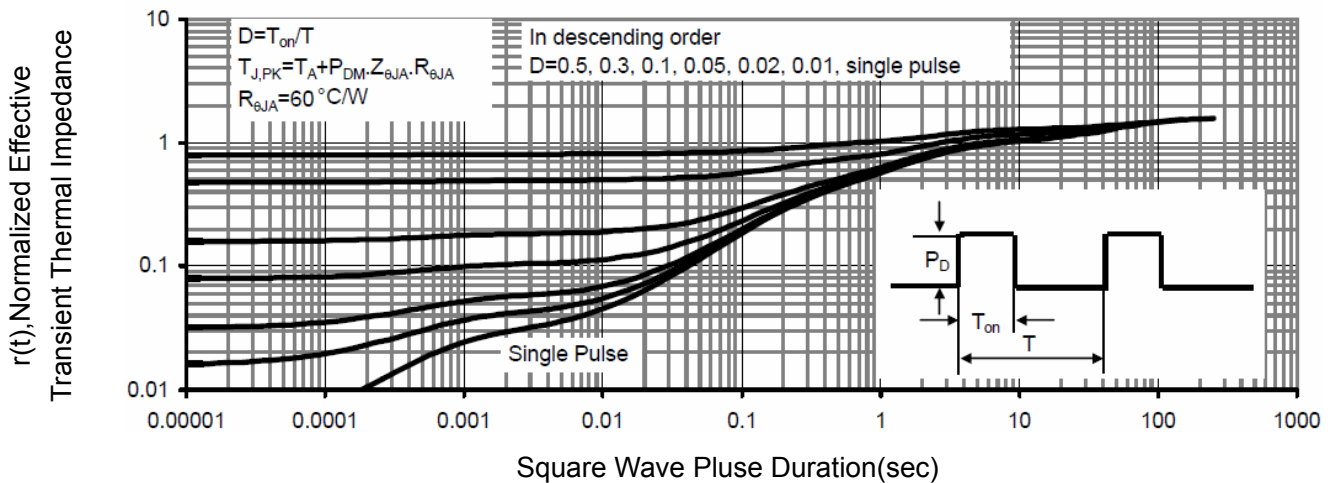
**Figure 9 Power De-rating**



**Figure 8 Safe Operation Area**

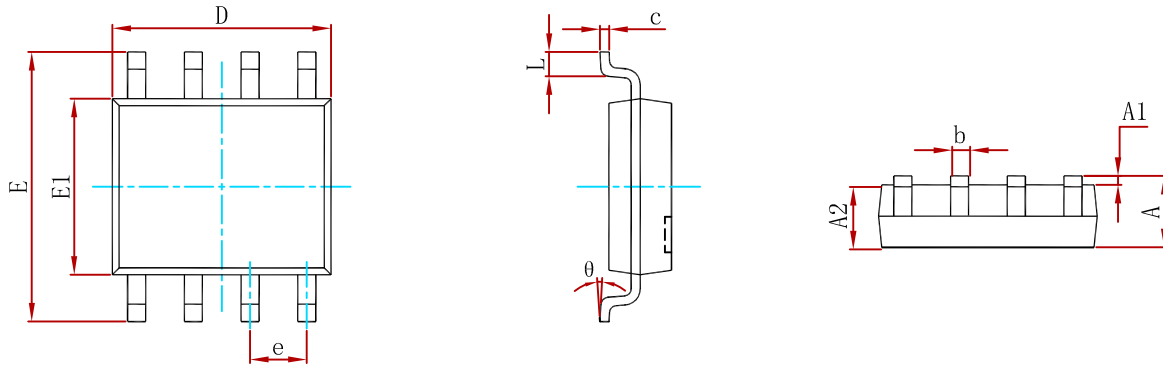


**Figure 10 Current De-rating**



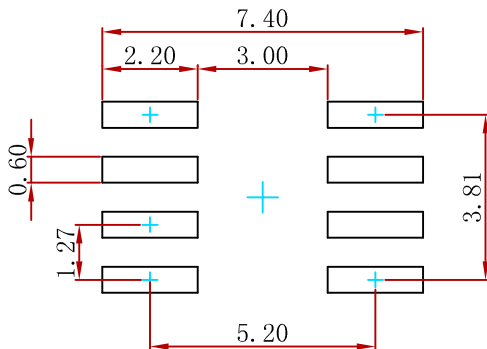
**Figure 11 Normalized Maximum Transient Thermal Impedance**

**PACKAGE MECHANICAL DATA**



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270 (BSC)		0.050 (BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

**Suggested Pad Layout**



Note:  
 1. Controlling dimension: in millimeters.  
 2. General tolerance: ± 0.05mm.  
 3. The pad layout is for reference purposes only.

**REEL SPECIFICATION**

P/N	PKG	QTY
AO4828-MS	SOP-8	3000

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